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Abstract - *This paper presents the design and the implementation of a fully monolithic coupled-oscillator array, operating at 6 GHz with close to zero coupling phase, in 0.25 µm BICMOS SiGe process. This array is made of four LC-NMOS differential VCOs coupled through a resistor. The single LC-NMOS VCO structure is designed and optimized in terms of phase noise with a graphical optimization approach while satisfying design constraints. At 2.5 V power supply voltage, and a power dissipation of only 125 mW, the coupled oscillators array features a simulated phase noise of -127.3 dBc/Hz at 1 MHz frequency offset from a 6 GHz carrier, giving a simulated phase progression that was continuously variable over the range* $-64° < \Delta\phi < 64°$ *and* $-116° < \Delta\phi < 116°$*. This constant phase progression can be established by slightly detuning the peripheral array elements, while maintaining mutual synchronization.*

Keywords – *coupled Oscillator, beam scanning, LC_NMOS VCO, BICMOS, phase noise.*

I. INTRODUCTION

Arrays of coupled oscillators are receiving increasing interest in both military and commercial applications. They are used to produce higher powers at millimeter-wave frequencies with better efficiency than is possible with conventional power-combining techniques [1]-[2]. Another application is the beam steering of antenna arrays [3-5]. In this case, the radiation pattern of a phased antenna array is steered in a particular direction through a constant phase progression in the oscillator chain which is obtained by detuning the free-running frequencies of the outermost oscillators in the array [3]. Also it is useful for automobile radar and communication systems applications [6].

Unfortunately, it is shown in [7] that the theoretical limit of the phase shift that can be obtained by slightly detuning the end elements of the array by equal amounts but in opposite directions is only ±90°. Thus, it seems to be interesting to study and analyze the behavior of an array of coupled differential oscillators since, in this case, the theoretical limit of the phase shift is within 360° due to the differential operation of the array. In this case, with the use of such an array, a continuously controlled 360° phase shifting range could be achieved leading to an efficient beam-scanning architecture for example [8]. Furthermore, differential VCOs are widely used in high-frequency circuit design due to their relatively good phase noise performances and ease of integration. The single integrated VCO performances in terms of tuning range, power dissipation and phase noise determine most of the basic performances of a complete array of coupled VCOs. As a consequence, the LC-VCO structure must be optimized. Furthermore, the use of a resistive coupling network instead of a resonant one can lead to a substantial save in chip area.

In this context, this work presents the design and the implementation of an original 6-GHz, low-phase noise and low-power array of four differential NMOS VCOs coupled through a resistive network using a 0.25 µm BICMOS SiGe process. The contributions of this work may be divided into two parts. The first part investigates the optimization and the implementation of the single integrated LC-VCO with an accurate graphical optimization method. The process of this optimization is performed through the minimization of phase noise while satisfying all different design constraints such as startup conditions, tank amplitude and tuning range. The second part of this work describes the design and the implementation of the four LC differential VCOs coupled through a resistor, to generate signals suitable for directly driving elements of a phased antenna-array.

This paper is organized as follows. Section II treats the circuit design with three subsections concerning the single VCO core design, the graphical optimization method used to minimize the phase noise and the post-layout simulation results of the optimized VCO in order to show the accuracy of the presented method. Section III presents the study, the implementation and the post-layout simulation results of the four NMOS differential VCOs coupled through a resistor, followed by the conclusion in Section IV.

II. SINGLE DIFFERENTIAL LC-VCO CIRCUIT DESIGN

A. The 0.25 µm RF-BICMOS SiGe Technology

Silicon Germanium (SiGe) is an emerging technology for use in radio frequency circuits. It offers low cost fabrication in conjunction with performance comparable to or better than III-V technologies for medium power applications. Because of this, SiGe is well suited for low cost applications with a high level of integration.

The VCO has been implemented in the NXP QuBIC4X 0.25µm BICMOS SiGe process on a p-type 200 Ω-cm Si substrate with five-level copper interconnect structure. Passive components including high-quality MIM capacitors are available in this process and inductors are designed using the top metal layer. The minimum physical gate length of the MOSFET's can be as low as 0.25 µm with an effective oxide thickness of 5.3 nm and a threshold voltage (V_T) of 0.61 V for NMOS transistors. The maximum supply voltage is 2.5 V. When transistor dimensions are scaled down, the RF performances are improved, mainly due to increased transconductance, gm, per unit width and less parasitic capacitances. The NMOS transistor can achieve a state of the art g_m and f_T of 1250 mS/mm and 137 GHz respectively.

This improvement in f_T and g_m will result in an increased switching speed for the VCO and reduced transistor noise figure. To design in this technology, MOS parameters which have been extracted from an earlier digital 0.25 µm BICMOS SiGe process have been used.

B. VCO core design

Fig. 1 shows the VCO schematic used and based on the well-known cross-coupled NMOS differential topology. The LC tank is made of a symmetric center-tapped inductor and a differentially tuned varactor. The cross connected NMOS differential pair provides the negative resistance to compensate for the tank losses. The tail current source is a simple NMOS current mirror. In these conditions, the width and the length of the NMOS tail transistor must be increased to reduce the flicker noise which lowers significantly the close-in phase noise of the VCO [9]. A tail capacitor C_T is used to attenuate both the high-frequency noise component of the tail current and the voltage variations on the tail node. This latter effect results in more symmetric waveforms and smaller harmonic distortion in LC-VCO outputs [10], [11]. Thus, the most significant remaining noise component of the tail current noise source is the up conversion of the flicker noise [12]. Large transistor channel length and widths are adopted to further suppress the flicker noise. A large size is possible since the tail source does not have to be a high speed device. Furthermore, this capacitor provides an alternative path for the tail current and, consequently, if the capacitor is large enough, the transistors of the differential pair might carry very little current for a fraction of the cycle leading to a class-C operation of the active part [12], [13]. Thus, the duty cycle of the drain current waveform is significantly reduced. This effect is

very important since it reduces the drain current noise injection during the zero-crossing of the tank differential voltage thus reducing significantly the phase noise due to the cyclostationary noise source of the active part as discussed in detail in [14].

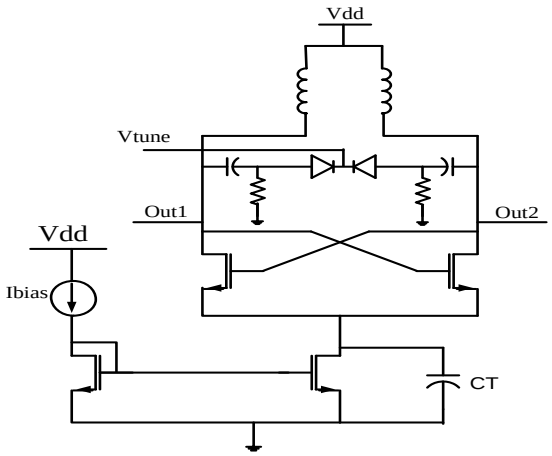


Figure 1. VCO schematic

The inductor is one of the most essential component in an LC-tank oscillator, since its quality factor affects the phase noise performances and determines the power dissipation. The inductor was implemented differentially and provides two advantages over its single-ended counterpart [15]. First, the differential inductor results in saving in chip area compared to two single-ended inductors. Indeed, two single-ended inductors must be placed sufficiently far apart so that their magnetic fields do not couple out of phase resulting in reduced inductance and hence a reduced quality factor. The second advantage is due to the mutual coupling between the two inductors. When the windings of the inductor are designed properly for a differential excitation, the magnetic fields add constructively resulting in an increase in inductance without a corresponding increase in the series resistance, this results in a higher inductor Q. Furthermore, it is now well known that a higher peak quality factor can be achieved by exciting an inductor differentially. This inductor was fabricated with the last metal level, which presents a low resistivity (12 mΩ/sq). The layout of the center-tapped inductor is shown in fig. 2 and fig. 3 shows its broadband three-port equivalent circuit model. The global value of the differential inductor was chosen to be 1 nH and the differential quality factor, given by (1), is evaluated and plotted in fig. 4.

$$Q_{diff} = \frac{\mathrm{Im}(Z_{11} + Z_{22} - Z_{12} - Z_{21})}{\mathrm{Re}(Z_{11} + Z_{22} - Z_{12} - Z_{21})} \quad (1)$$

Where Z_{11} is the circuit input impedance; Z_{12} is the open Circuit Transfer impedance from port 1 to port 2; Z_{21} is the open Circuit Transfer impedance from port 2 to port 1 and Z_{22} is the open circuit output impedance.

As shown in this figure, the associated differential Q factor of the symmetric center-tapped inductor is equal to 22 at 6 GHz. Let us note that we consider here that the inductor has been designed in order to obtain a maximum Q factor at 6 GHz i.e. the geometric parameters, b, s, n and d of the inductors are chosen so that the equivalent parallel conductance, g_L, becomes minimum for this value of L, thus maximizing the quality factor Q. The supply voltage Vdd is injected via the middle terminal and is brought around the outside of the inductor to reach the Vdd pad and maintain symmetry. This additional metal is of no consequence and does not contribute to the tank inductance or resistance because the middle terminal is forced to be a virtual ground as a result of the differential excitation [16].

It is shown in [17] that an increase in Q-values for inductors, partly depending on technology improvements and partly due to better optimization algorithms can be obtained. The Q-values of the tank is now not always dominated by the Q-value of the inductor, and as the inductor losses decrease, more focus must be set on the varactor design, especially for high frequency circuit designs.

For this design, varactor diodes have been used as its Q-value shows less variation over the tuning range than the MOS-varactors used in inversion mode. The simulated Q-value of the chosen varactor is presented in fig. 5. The Q-value varies from 27 to 55 over the tuning range (0 V- 2.5 V), at a 6 GHz frequency.

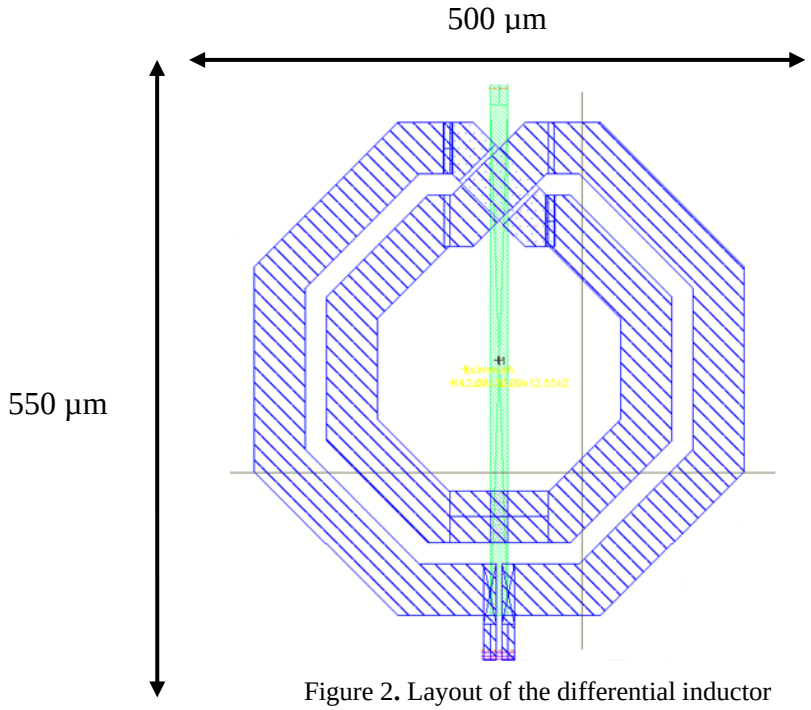


Figure 2. Layout of the differential inductor

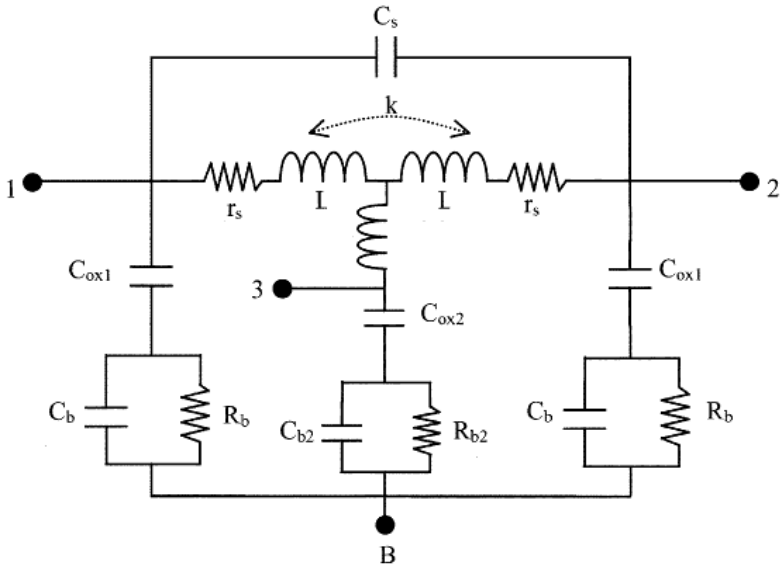


Figure 3. Lumped circuit model of the differential inductor

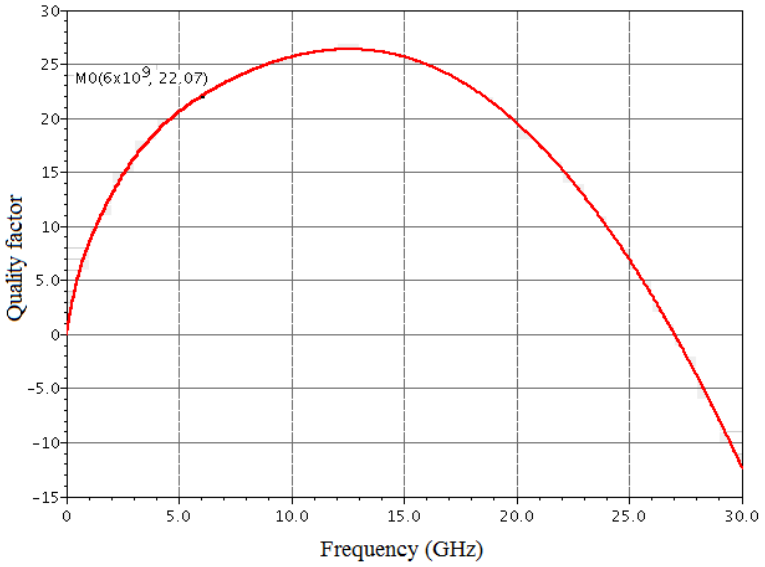


Figure 4. Simulated Q factor of the differential inductor

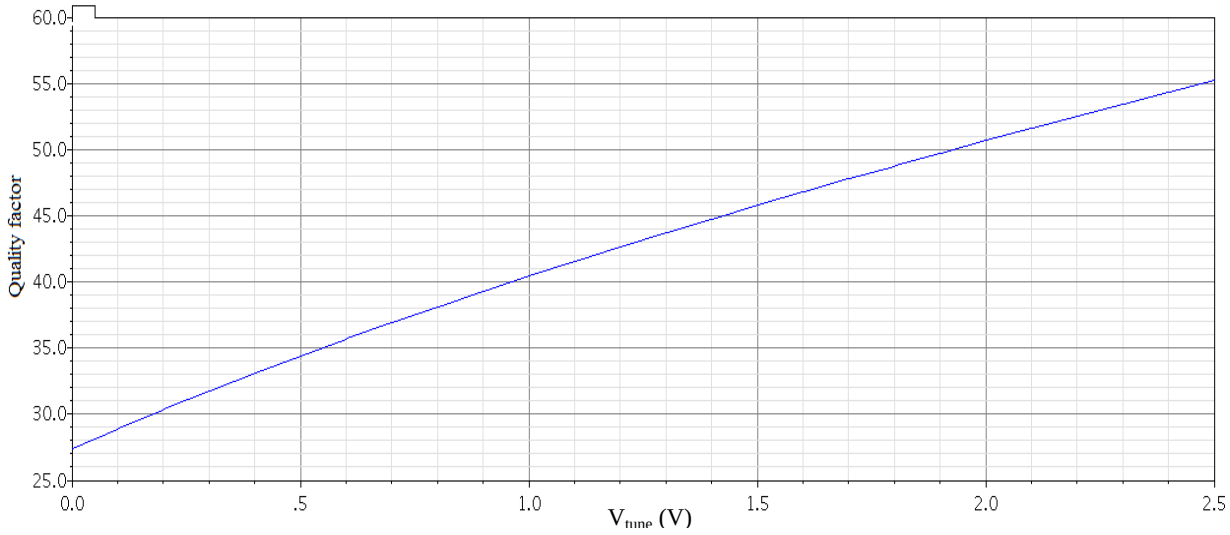


Figure 5. Simulated Q factor of the varactor

C. Optimization approach

The past 20 years have seen significant progress in the understanding of noise in electrical oscillators. During this period, recent work by Bank, Mazzanti and Andreani has offered a general result concerning phase noise in nearly-sinusoidal inductance-capacitance (LC) oscillators [18]. Central to Hajimiri and Lee's work is the derivation of the impulse sensitivity function (ISF) that shows how the phase disturbance produced by a current impulse depends on the time at which the impulse is injected. The work is very intuitive and, if applied correctly, results in accurate predictions; notably Andreani et al. [19]-[22] have used the ISF to develop closed form expressions for the most common inductance-capacitance (LC) oscillators. With only few steps, this can predict phase noise in a range of popular oscillator circuits and guide their optimal design. Furthermore, Hajimiri & al present in [23] an effective graphical method to visualize the design constraints such as tank amplitude, frequency tuning range, and startup condition, allowing minimization of phase noise while satisfying all these design constraints. Nevertheless, in [23], the bias current of the VCO, which is an important parameter for the phase noise optimization, is chosen arbitrary to the maximum current allowed by the specifications. This choice does not constitute an optimal optimization strategy. Indeed, let us remind that a simplified and widely used phase noise model separates the amplitude behavior versus the bias current into two operation modes named voltage and current-limited regimes [24].

Thus, the phase noise decreases in the first regime until it reaches the stable transition point located between the two regimes. So, the desired bias current point for the optimum phase noise and power consumption performances is located at the intersection of these two regimes. Due to this considerations, the method presented by Hajimiri has been improved by adding a particular technique based on the obtaining of the optimum bias current of the VCO using a three dimensional phase noise representation using a parametric analysis and then, starting from this optimal current, to use the graphical optimization method proposed in [23] and adapted to our 6 GHz NMOS only LC VCO architecture. This process of modelization and optimization of the LC-VCO topology is used in [25] but the LC VCO topology is different from that used in our case which leads to a new modeling of the VCO and a new writing of the equations defining the design constraints.

Hence, for this LC VCO architecture, the adopted optimization methodology which is based on the following steps is detailed:

- Specifications definition ;
- VCO model determination ;
- Optimum Bias conditions determination ;
- Phase noise graphical optimization ;
- Phase noise estimation using the optimum parameter found in the previous step.

The first step of the optimization approach is to model the various VCO components. Using the model presented in [26] and illustrated in Fig.6, the effective parallel equivalent conductance of the inductor, g_L, is given by:

$$g_L = \frac{1}{R_p} + \frac{R_S}{(\omega L)^2} \tag{2}$$

where R_p and R_s represents the parasitical elements of the inductance.

The effective parallel equivalent varactor conductance, g_v, used is then given by:

$$g_V = \frac{1}{R_V} = \frac{C_V \omega}{Q_V} \tag{3}$$

Where R_v is the varactor diode parasitic serie resistance and Q_v represents the quality factor of the varactor.

Furthermore, the very useful NMOS transistor analytical model described in [26] is used for the graphical optimization and visualization of design constraints.

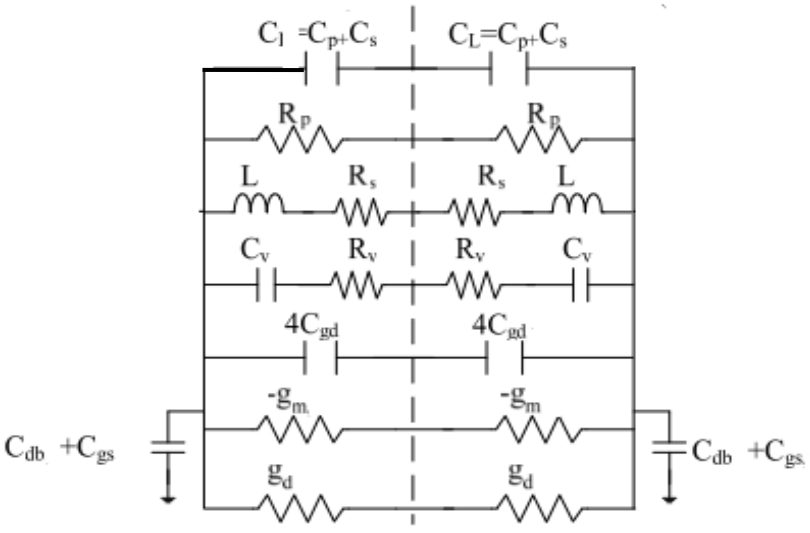


Figure. 6. Equivalent oscillator model

Let us note that in Fig.6, g_m and g_d are small-signal transconductance and output conductance of the transistors respectively. Although the values of g_m and g_d vary with the change of the operating points of the transistors in the course of oscillation, we will use the values of g_m and g_d corresponding to a voltage across the LC tank of zero. This approximation facilitates the analytical expression of design constraints [23].

To minimize the phase-noise, the minimum tank inductance for oscillator start-up was found and the current was maximized, but limited, so that the RF voltage swing does not saturate the transistor. Thus, the VCO is operating in a current limited regime and any further increase in current would be wasted because the transistor would saturate. Saturating the transistor would drive the oscillator into the voltage limited regime and there would not be any further decrease in phase noise for an increase in current. So, the desired bias current point for the optimum phase noise and power consumption performances is located at the intersection of the two regimes (voltage and current limited regime). Due to these considerations, the aim of this method is first to determine the optimum bias current of the VCO using a three dimensional phase noise representation using a parametric analysis and second, starting from this optimal current, to use the graphical optimization method proposed in [23] adapted to our 6 GHz NMOS only LC VCO architecture.

For the determination of the optimum bias current of the VCO minimizing the phase noise, we exploit the following expression describing the VCO phase noise model (pn) [25].

$$Pn(f_{offset}) = \left[\frac{1}{16\pi^2 f_{offset}^2} \cdot \frac{L^2 (2\pi f_0)^2}{V_{tank}^2} \right] \left[2kT(g_L + g_v + \gamma g_d \right] \quad (4)$$

Where k is the Boltzmann constant, T is the temperature, V_{tank} is the oscillation amplitude, f_0 is the oscillation frequency, f_{offset} is the offset frequency from the carrier, γ is equal to 5/2 and g_d is the output conductance.

So, for each value of I_{bias}, the tank voltage and the phase noise are calculated using (4). Fig. 7 shows a three-dimensional representation of the LC-VCO phase noise. In this figure, the (x-y) plane describes the bias conditions of the VCO and the z-axis corresponds to phase noise prediction. Thus, an initial optimal bias condition for which the phase noise is estimated to be at the minimum is selected. The coordinates of this minimum for this 6-GHz VCO is given by: I_{bias} = 14.6 mA and *P*n (1 MHz) = -122.43 dBc/Hz.

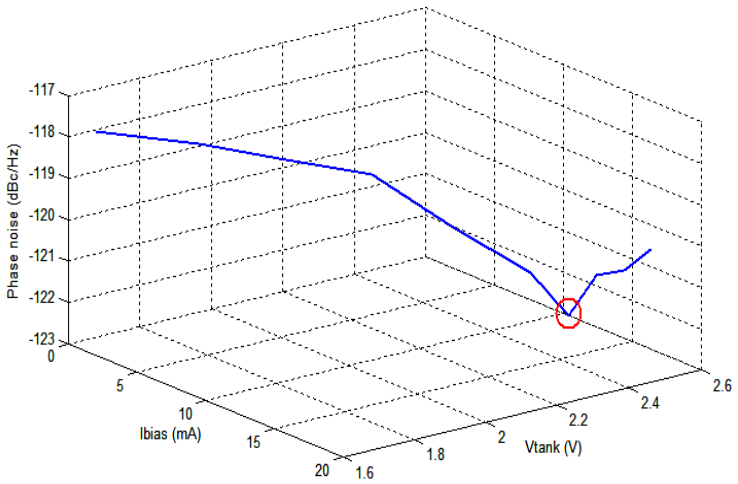


Figure 7. Calculated phase noise versus V_{tank} and I_{bias}

Fig. 8 shows the corresponding V_{tank} versus I_{bias} characteristic. Under the optimum bias situation, the oscillator should operate at the verge of the I-limited regime and the V-limited regime. This design strategy will be executed using a graphical optimization method while satisfying all the design constraints, as shown in the following.

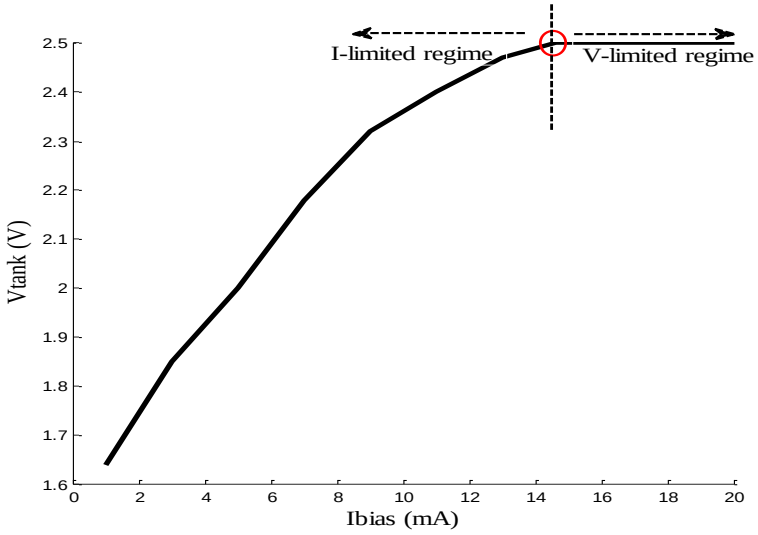


Figure 8. The V_{tank} versus I_{bias} characteristic of the VCO core

The second step of the optimization process, after the bias condition selection, consists in the representation of the design constraints in the variable plane. The initial design variables are listed in Table 1, which includes the geometric parameters of the on-chip spiral inductor, the MOS transistors dimensions (W_n and L_n) and the maximum and minimum values of the varactor capacitance ($C_{v,max}$ and $C_{v,min}$).

Table 1. Initial design variables

Components	***Initial design variables***
Transistors	W_n, L_n
Spiral inductor	b, s, n, d
Varactors	$C_{v,max}$, $C_{v,min}$

The number of these design variables can be reduced as explained in the following: first, the geometric parameters of the inductor are fixed in order to obtain a high inductor quality factor as mentioned previously. Second, the channel length L_n is set to the minimum allowed by the process technology for maximum transition frequency (F_T) and transconductance g_m. Third, the ratio $C_{v,max}/C_{v,min}$ is maximum. Therefore, the varactor introduces only one design variable ($C_{v,max}$).

Finally, we reduce the number to only two design variables, as shown in Table 2, the transistors width W_n and the maximal varactor capacitance $C_{v,max}$ which will be referred to C in the following. Consequently, the design constraints will be represented in the (W_n, C) plane as shown in figure 9.

Table 2. Reduced design variables

Components	***Reduced design variables***
Transistors	W_n
Varactors	$C_{v,max}$

These design constraints are imposed on tank amplitude, power dissipation, frequency tuning range and startup conditions.

In these conditions, and in order to ensure a large enough voltage swing, the tank amplitude is required to be larger than $V_{tank,min}$ so that:

$$V_{\text{tank}} = \frac{I_{bias}}{g_{\text{tank, max}}} \geq V_{\text{tank, min}} \tag{5}$$

Where $V_{tank,min}$ is chosen to be equal to 1 V and $g_{tank,max}$ is the maximum tank conductance.

Moreover, the startup conditions with a small-signal loop gain of at least σ_{min} are fixed by:

$$g_{active} \geq \sigma_{\min} g_{\text{tank,max}} \tag{6}$$

Where $2g_{active} = g_m$ and $2g_{tank} = g_d + g_v + g_L$ with g_m and g_d the small-signal transconductance and output conductance of the NMOS transistors respectively. The worst-case conditions is imposed by $g_{tank,max}$. To overcome the possible error that the approximation for g_m mentioned previously might cause, we can select a conservative minimum small-signal loop gain σ_{min}=3.

Finally, the oscillation tuning range is limited by two values depending on the center frequency ω_0, so that:

$$L_{\text{tank}} C_{\text{tank, min}} \leq \frac{1}{\omega_{\max}^2} \tag{7}$$

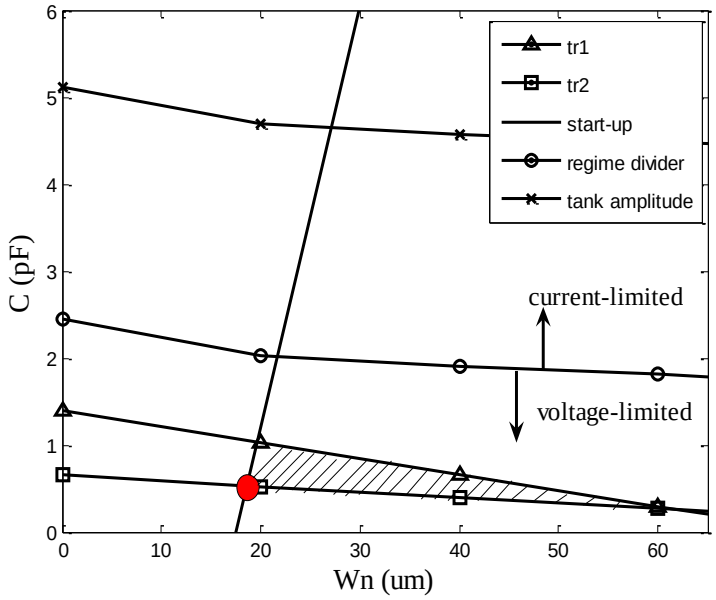
$$L_{\text{tank}} C_{\text{tank, max}} \geq \frac{1}{\omega_{\min}^2} \tag{8}$$

The design constraints given by (5) to (8) are expressed and formulated as functions of W_n and C variables. Then, a program which allows to calculate, for each value of the transistor width, the varactor capacitance C so that the design constraints are fulfilled, was developed. The associated curves are shown in fig. 9(a), using the initial I_{bias} condition already determined (I_{bias} =14.6 mA).

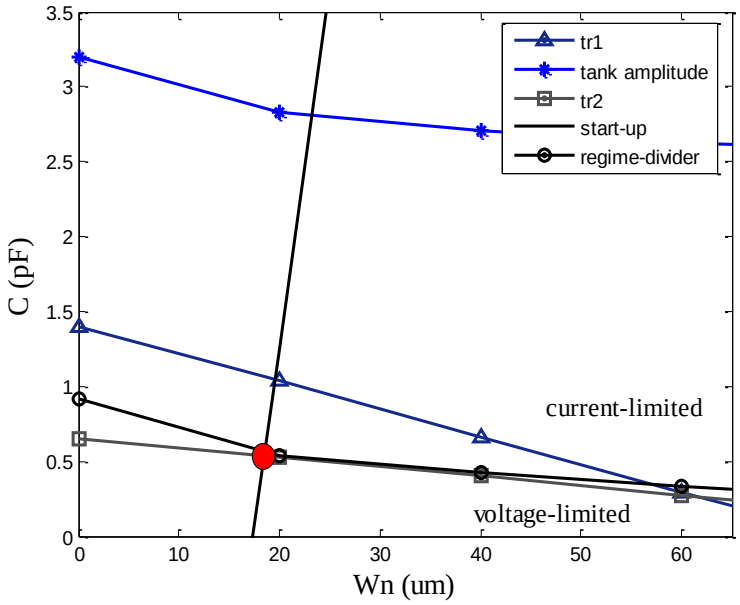
The region below the tank amplitude line corresponds to V_{tank} larger than 1 V. Below the regime-divider line, the oscillator operates in the V-limited regime. The tr_1 and tr_2 lines represent the upper-limit and the lower-limit of tuning range, respectively. Tuning range is achieved if the region lies between the tr_1 and tr_2 lines. On the right-hand side of the startup line, oscillation is guaranteed [23] meaning that the small-signal loop gain is over σ_{min}=3 on the right-hand side of the startup line. Hence, this value of σ_{min} takes into account a margin for the VCO starting condition.

The region with shadow in fig. 9(a) satisfies all the design constraints and represents a set of feasible design points. The optimum point is defined by the intersection of the startup line and tr_2 line since this point corresponds to the lower parasitic capacitances values. However, we can notice that the optimum point is located in the voltage limited regime (below the regime divider). Therefore, the design suffers from waste of power. As a consequence, the bias current must be reduced until the optimum is located on the regime divider line. In this case, fig. 9(b) shows the optimum design with I_{bias}=12.2 mA for which no further action is necessary.

As a consequence, the obtained optimum point is defined by: Wn =20 µm ; C = $C_{v,max}$ = 0.6 pF and I_{bias} = 12.2 mA.



(a)



(b)

Figure 9. Design constraints visualization for: (a) I_{bias} =14.6 mA; (b) I_{bias} = 12.2 mA

D. Implementation and post layout simulation results

The 0.25 µm BICMOS SiGe process described in section II.A is used to implement the VCO. The layout of the LC-VCO is shown in fig. 10. The symmetry of the layout is important in order to maintain the wave-form symmetry which plays an important role in conversion of noise to phase noise. Good matching of the transistors is also important to maintain good differential outputs with amplitude and phase matching. The LC-VCO layout area is 525*860 µm². Multi-finger structures are used for the NMOS transistors as well as for the varactors.

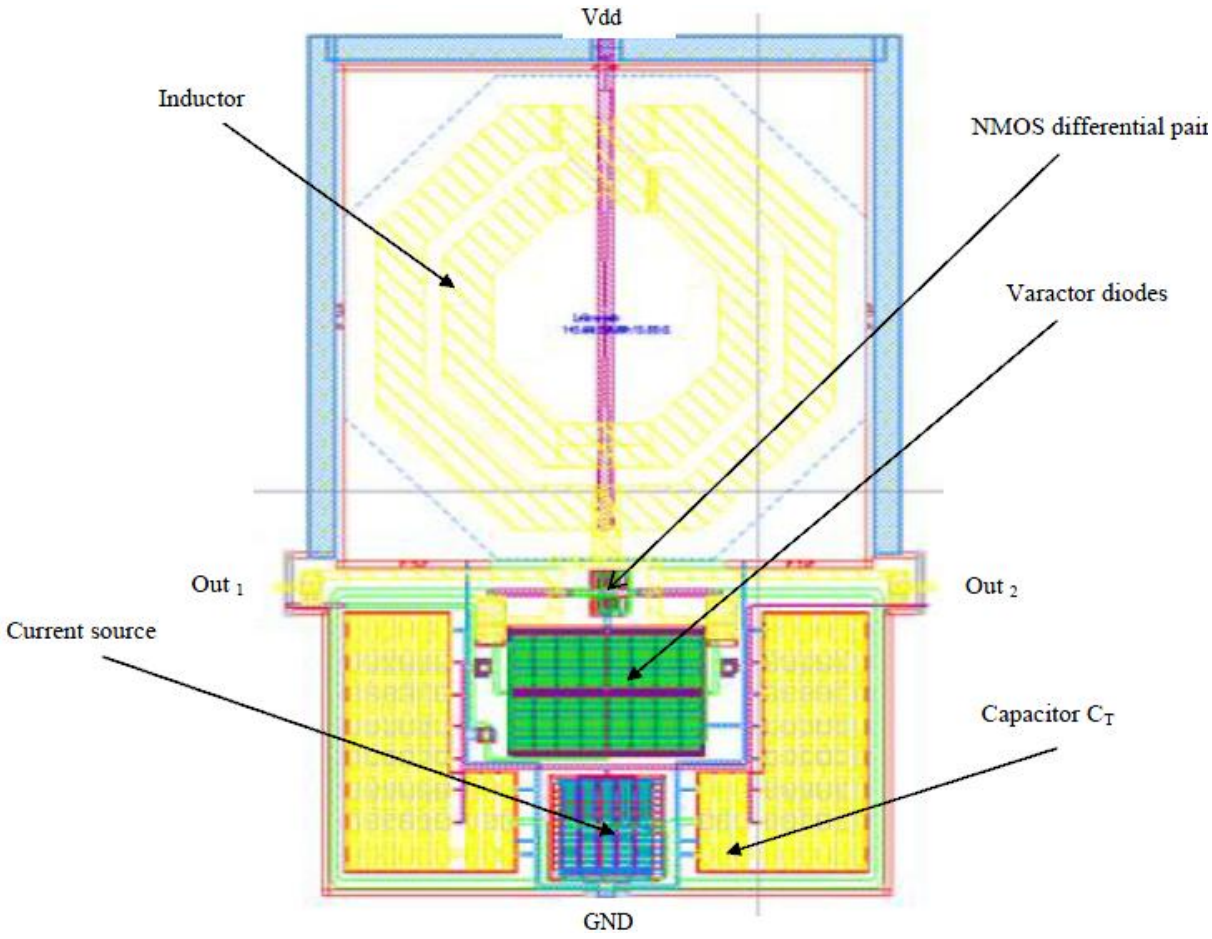


Figure 10. LC-VCO Layout

Several simulations have been performed with Spectre RF, in order to assess the performances of the proposed LC-VCO design. The tuning characteristic of the VCO is presented in fig. 11. The VCO can be tuned from 5.95 GHz to 6.38 GHz with a tuning voltage varying from 0 to 2.5 V. Fig. 12 shows the plot of the post-layout simulated phase noise at 1 MHz frequency offset versus the tuning voltage and fig. 13 shows the plot of the phase noise versus frequency offset for a tuning voltage of 0 V. As can be seen on these two figures, the VCO features a worst case phase noise of –120.65 dBc/Hz at 1 MHz frequency offset under 2.5 V power supply voltage. So, the worst case FOM calculated using (9) is equal to -181.2 dBc/Hz.

$$\mathrm{FOM} = \mathrm{L}\{\Delta f\}[\mathrm{dBc/Hz}] + 10\log\left(\mathrm{P_{DC}}[\mathrm{mW}]\right) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) \tag{9}$$

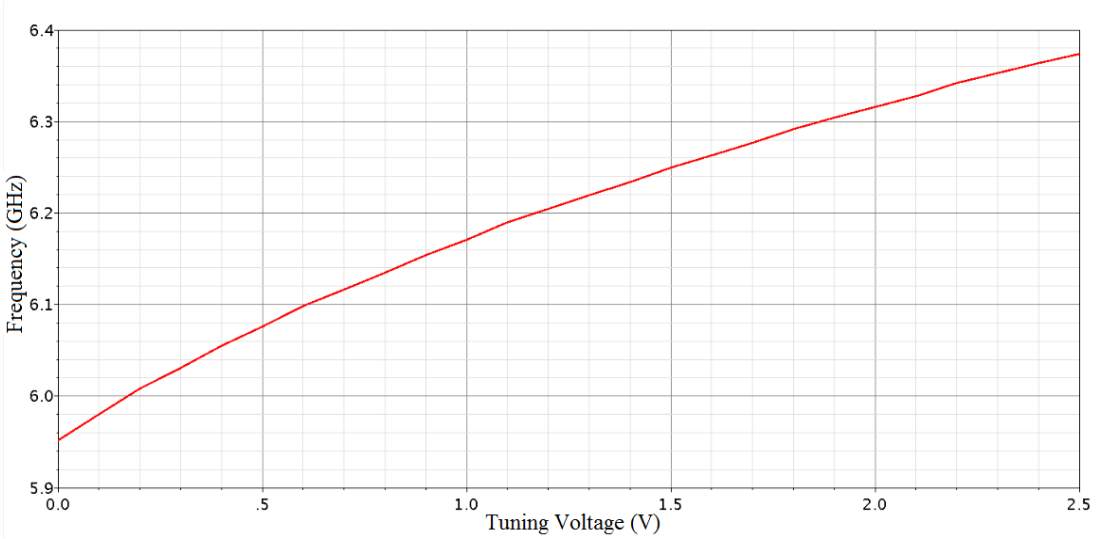


Figure 11. Tuning characteristic of the NMOS LC VCO

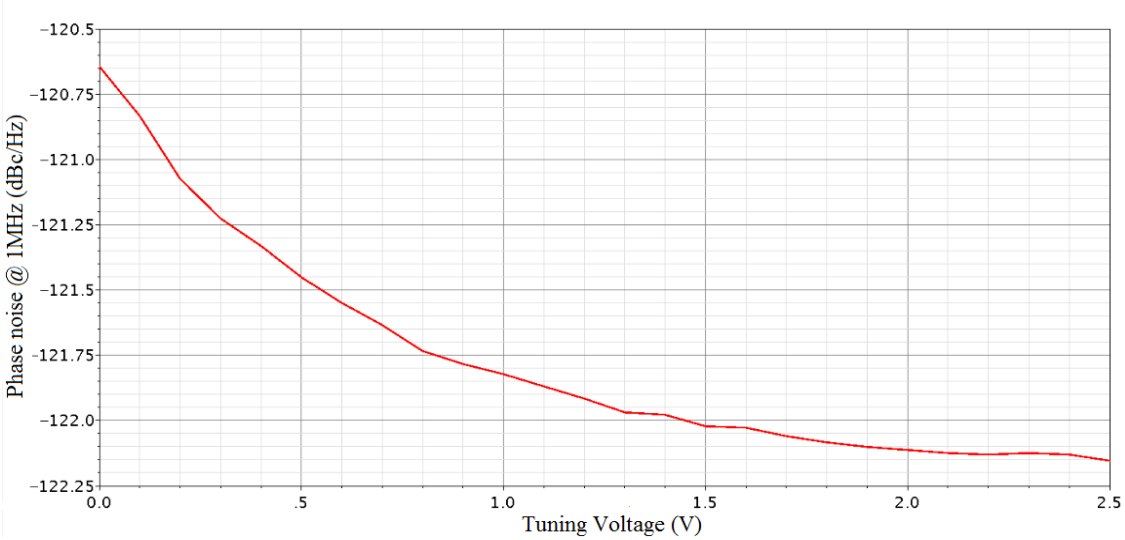


Figure 12. Simulated phase noise at 1MHz frequency offset versus tuning voltage.

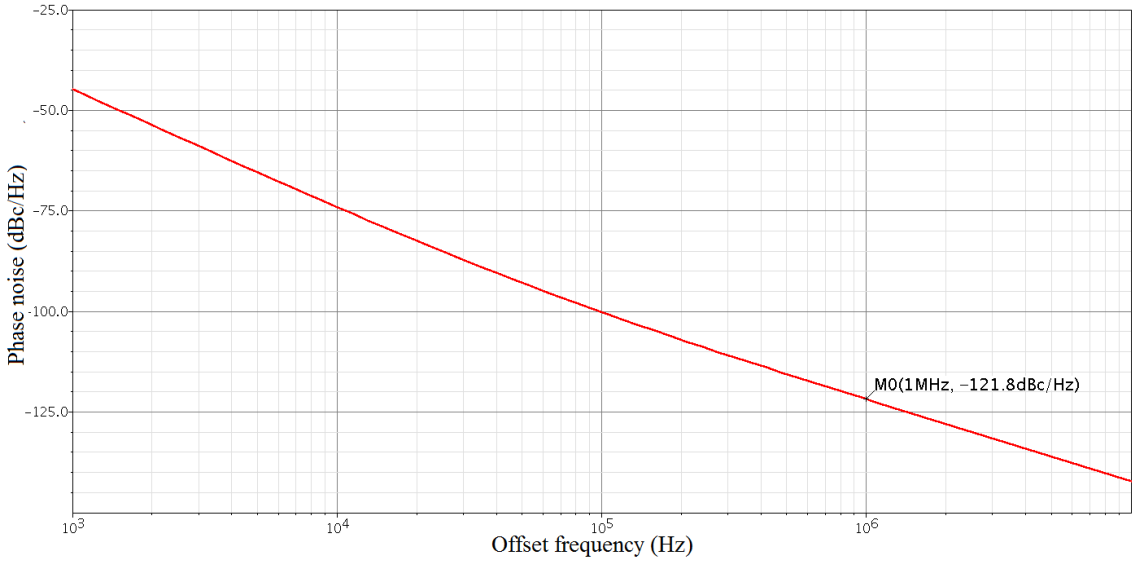


Figure 13. Simulated phase noise of the VCO for a tuning voltage of 0.9 V.

In order to verify the accuracy of the presented graphical optimization method, table 3 presents a comparison between theoretical (presented method) and post-layout simulation (Spectre RF software) results. Let us note that the theoretical phase noise value is calculated using (4) after optimization and the simulated phase noise is obtained for Vtune = 0.9 V (i.e. C = 0.6 pF). As we can see, a good agreement was found between theoretical and simulated results.

Table 3. Comparison between theoretical and post layout simulated results

	Graphical Optimization	*Spectre RF Software*
Frequency (GHz)	6	6.15
Tuning range (%)	10	8.9
Phase noise(dBc/Hz)	-122.44	-121.8

The simulated performances of this 6-GHz fully integrated NMOS differential LC VCO are summarized in Table 4.

Table 4. 6-GHz VCO Post layout Simulated performances Summary

Supply Voltage (V)	**2.5**
Power consumption (mW)	**31.25**
Area (μm^2)	**525*860**
Tuning Range (MHz)	**450**
Tuning Voltage (V)	**0- 2.5**
F_0 (GHz)	**6.15**
Phase Noise @ 1 MHz (dBc/Hz) at 6.15 GHz	**-121.8**
Phase Noise @ 1 MHz (dBc/Hz) at 5.95 GHz	**-120.65**
Worst case FOM at 5.95 GHz (dBc/Hz)	**-181.2**

III. DESIGN AND IMPLEMENTATION OF AN ARRAY OF FOUR COUPLED DIFFERENTIAL VCOs

A. Coupled oscillator arrays

The study of the synchronization of oscillators started with B. Van der Pol [27] who used an "averaging" method to obtain approximate solutions for quasi-sinusoidal systems. Then, R. Adler gave to the microwave oscillator analysis a more physical basis defining the phase dynamic equation of an oscillator under the influence of an injected signal [28]. This was sustained by K. Kurokawa who derived the dynamic equations for both the amplitude and phase [29], providing a pragmatic understanding of coupled microwave oscillators. These methods were generalized by R. York to include any number of oscillators coupled via a coupling circuit, first broadband [30], and then narrow band [31].

Independently of the topology, an oscillator array must satisfy two requirements: First, the basic oscillators must synchronize at a common frequency. Second, they must maintain the phase difference between them to the required value. The most challenging task is to ensure and control precisely this proper phase difference. This requires an understanding of the influence of various circuit parameters such as coupling strength and the oscillators tunings for many practical combinations of each. When

the free-running frequencies of the oscillators are within a collective locking-range, the oscillators will spontaneously synchronize with a phase relationship that is controlled by the original distribution of free-running frequencies [3], [7]. Furthermore, it is shown that a constant phase progression can be established along the array simply by selecting properly the free-running frequencies.

This later solution is established by setting all of the free-running frequencies of the central-array elements to a common center frequency and slightly detuning the peripheral elements in proportion to the amount of the desired inter-element phase shift. The resulting phase shift is then independent of the number of oscillators in the array [32]. The uniform phase distribution is a common design objective, and potentially useful for beam scanning or power combining.

Furthermore, a phase noise analysis near the carrier in coupled-oscillator arrays with zero phase progression has been performed for a few common coupling topologies in [33] , [34] and [35]. This analysis shows that the total phase noise of the array is significantly reduced compared to that of a single free-running element in the array in direct proportion to the number of array elements, provided the coupling network is designed properly. Hence, the total phase noise of N coupled differential oscillators is reduced by 1/N, independent of the phase progression along the array, so that:

$$pn(dB)_{total} = -10LogN + pn(dB)_{\text{single}} \tag{10}$$

Where $pn(dB)_{total}$ is the total phase noise of the coupled differential VCOs, N is the number of array element and $pn(dB)_{single}$ is the phase noise of the single VCO.

The designed array consists in four NMOS differential VCOs coupled through a resistor as shown in fig. 14. Let us note that each VCO in the array is assumed to be designed and optimized using the method presented in section II. Furthermore, the VCOs are considered identical, except for their free-running frequencies or tunings. Thus, the four VCOs of the array can be tuned using the control voltages $Vtune_1$, Vtune and $Vtune_4$.

Furthermore, as mentioned previously and according to York & al., the inter-stage phase shift is independent of the number of oscillators in the array and can easily be controlled by slightly detuning the free-running frequencies of the two outermost VCOs in the array. As a consequence, the desired synchronization frequency is imposed to the VCOs 2 and 3 via the tuning voltage Vtune whereas the tuning voltages of the two outermost VCOs ($Vtune_1$ and $Vtune_4$) can be adjusted in order to obtain the desired phase shift using the CAD tool proposed in [36].

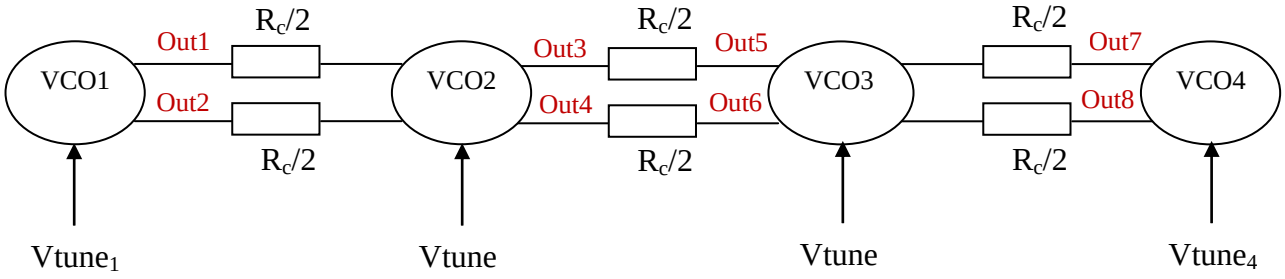


Figure 14. The linear array of four coupled VCOs.

B. Implementation and post layout simulation results

The coupled-oscillator array was also implemented in the NXP QuBIC4x, 0.25 µm SiGe process described in section II.A. The layout of the array is shown in fig. 15 and occupies an area of 4 mm^2 (pads included).

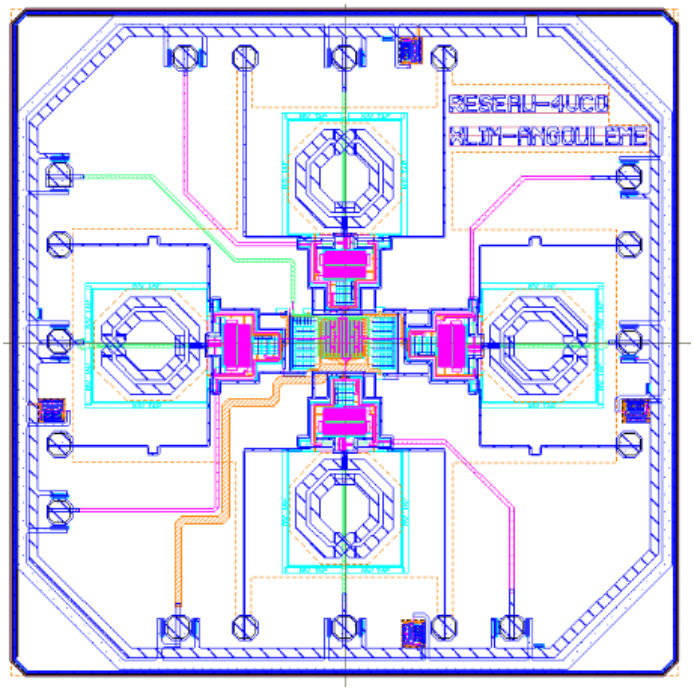


Figure 15. Layout of the array of four coupled differential VCOs.

The four differential VCOs were coupled through a resistor of 400 Ω, in order to maximize the locking range as well as the phase variation according to [8, 30].

Post-layout simulations, performed with Spectre RF, show that the minimum value of the phase shift between adjacent VCOs was found to be equal to 0.85° and is obtained for free-running frequencies f_{01} = f_{02} = f_{03} = f_{04} = 6.15 GHz. Fig. 16 shows the four sinusoidal waveforms with an amplitude of 18 mV at the output of each VCO on 50 Ω load. In this case, the four coupled oscillators are synchronized at 6.15 GHz.

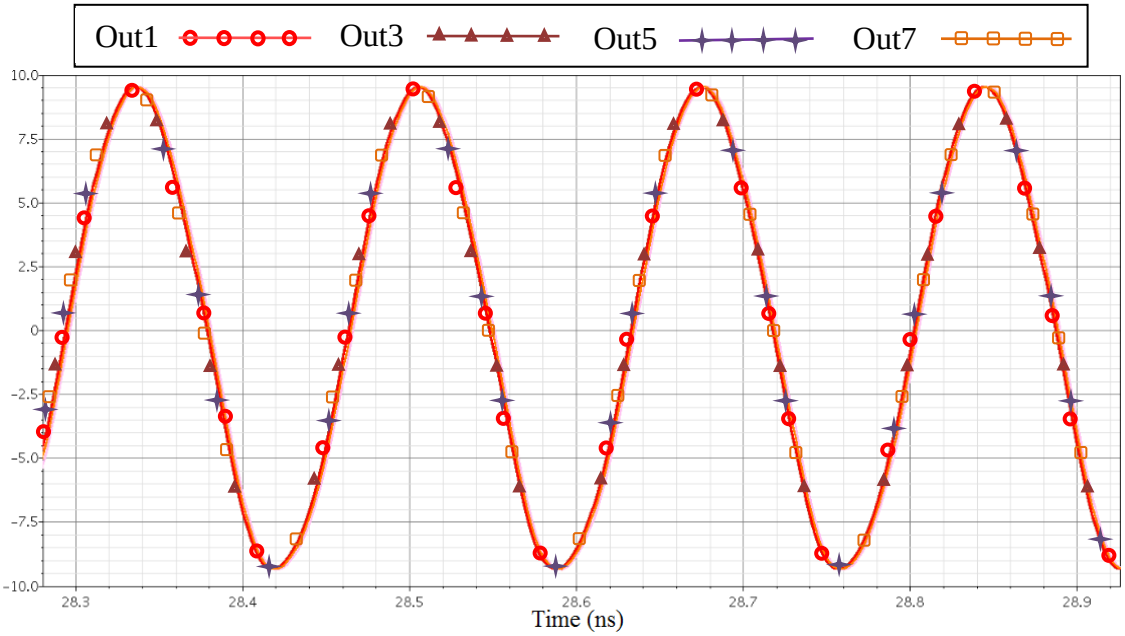


Figure 16. Output voltages of the coupled differentials VCOs when f_{01}= f_{02}= f_{03} = f_{04} = 6.15 GHz.

Now, in order to show the ability of the system to achieve the desired phase shift, we changed the free-running frequencies of the two outermost VCOs of the array (VCO1 and VCO4) so that the synchronization frequency will remain the same (i.e. 6.15 GHz). An example of the output waveforms of the four coupled VCOs is shown in Fig. 17. In this example, the post layout simulated phase shift is

28.24° between out 1 and out 3, 29° between out 3 and out 5 and finally 28.8° between out 5 and out 7. This phase shift is obtained for f_{01}= 6.22 GHz, f_{02} = f_{03} = 6.15 GHz and f_{04} = 6.08 GHz. Let us note that the maximum value of the phase shift is obtained for f_{01}= 6.27 GHz , f_{02}= f_{03} = 6.15 GHz and f_{04} = 6.03 GHz and is equal to 64°. Above this values of the free-running frequencies, the VCOs are not able to synchronize anymore.

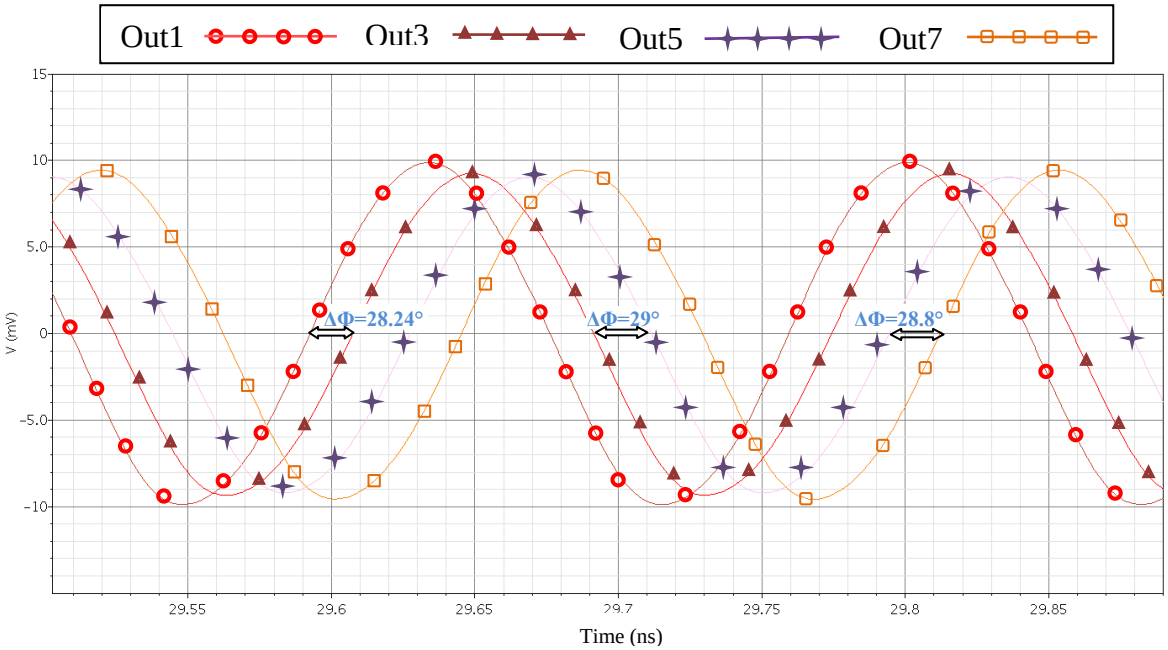


Figure 17. Output voltages of the coupled differentials VCOs for f_{01}= 6.22 GHz; f_{02}= f_{03} = 6.15 GHz and f_{04}= 6.08 GHz with Δϕ= 29°.

Furthermore, Fig.18 shows the variations of the post-layout simulated phase shift Δϕ between the four coupled VCOs as a function of Δf_0 where $\Delta f_0 = f_{01}-f_{04}$ with f_{01} and f_{04} the free running frequencies of VCOs 1 and 4 respectively.

As can be seen on this figure, as the VCO tunings are moved apart so that the synchronization frequency will remain the same (i.e. for $\frac{f_{01}+f_{04}}{2}=6.15GHz$), the phase shift increases until the locking-region boundary is encountered. Moreover, one can notice that the inter-stage phase shift varies continuously from -64° to 64°. Nevertheless, due to the differential operation of the array, one can obtain also a constant phase progression varying from -116° to 116° as shown in Fig. 18.

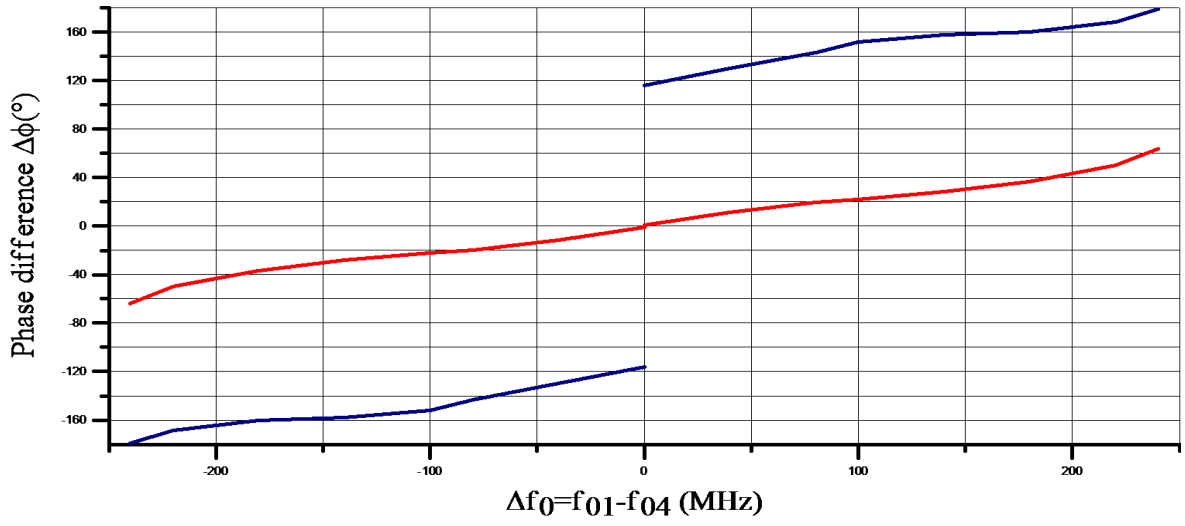


Figure 18. Phase difference Δϕ versus Δf_0.

The phase difference obtained is necessary for the beam steering of antenna arrays. To obtain an agile and electronically beam steering, it is essential to master the phases of the signals applied on each elementary antenna. For a linear array, a phase shift $\Delta\phi$ between adjacent elements results in steering the beam to an angle θ_0 off broadside, given by [37]:

$$\theta_0 = \arcsin\left(\frac{\lambda}{2\pi d}\Delta\phi\right) \tag{11}$$

where d is the distance separating two antennas and λ is the free-space wavelength.

As expected, the radiation angle depends on the relative phase shift applied between two adjacent elements. In our case, the radiation pattern of the phased antenna array can be steered in a particular direction by establishing a constant phase progression throughout the oscillators chain. Fig. 19 shows the phase shift to be imposed between adjacent VCOs controlling the antenna-array elements for a distance d between antennas equal to $\lambda/2$. It should be noted that a zero phase shift implies a radiation direction $\theta_0 = 0°$. Furthermore, the radiation angle varies between ± 90 ° for a phase difference varying from –180° to +180 °. With the presented circuit, the limit of the phase shift is only ± 64 ° but due to the differential nature of the array, the region between -180 ° and -116 ° and between +116° and +180° can be controlled which is not possible without the use of an array made of differential VCOs.

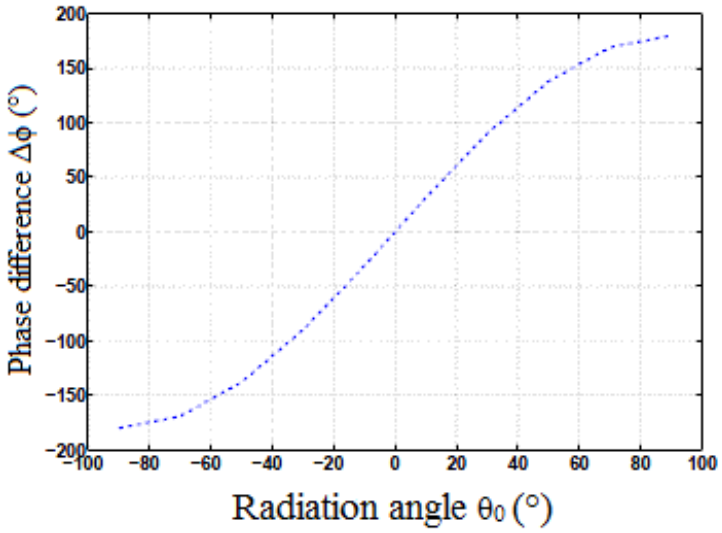


Figure 19. Phase difference $\Delta\phi$ versus the radiation angle θ_0 for $d=\lambda/2$.

Thus, these results show that it is possible to adjust, with a relatively high accuracy, the free-running frequencies of the four differential NMOS VCOs required to achieve the desired phase shift necessary for electronic beam steering in linear antenna arrays.

Fig. 20 shows the post-layout simulated phase noise of the total array output under synchronized conditions for the following free-running frequencies of the VCOs : f_{01}= 6.13 GHz ; f_{02}= f_{03} = 6.15 GHz and f_{04} = 6.17 GHz. The coupled oscillators array features a worst case phase noise of -127 dBc/Hz @ 1 MHz frequency offset.

Figure 20. Simulated phase noise of the array for $\Delta\phi = 23°$.

Let us remind that the individual array elements feature a single sideband phase noise of -121.8 dBc/Hz at 1 MHz frequency offset for V_{tune} = 0.9 V. In the same conditions, i.e. for $Vtune_1$ = Vtune = $Vtune_4$= 0.9 V, the array of four VCOs features a phase noise equal to -127.3 dBc/Hz. As a consequence, the simulation shows a good qualitative agreement with the theory since the total phase noise of four coupled VCOs is reduced by -10 log 4 (i.e. 6 dB) compared the phase noise of one single VCO. Furthermore, figure 21 shows that the total phase noise of the array varies between -127.3 and -127 dBc/Hz and hence, can be considered independent of the phase shift along the array.

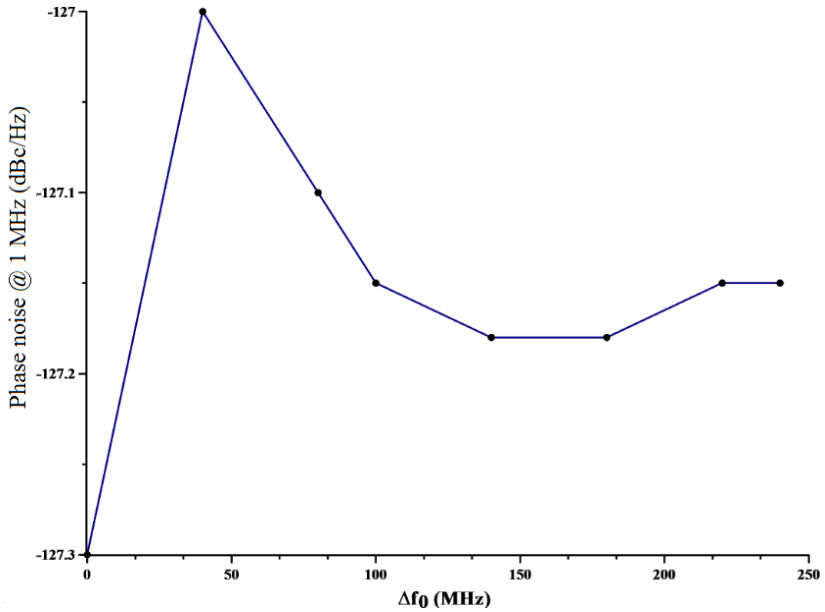


Figure 21. Post layout simulated phase noise of the array at 1 MHz frequency offset versus Δf_0.

Furthermore, let us remind that in an integrated circuit, a gradient in the silicon process can lead to a difference between the coupling resistors. Therefore, the phase shift behavior in the case of such a mismatch between the resistive network can be an important issue. So, in order to verify the robustness of our array of differential coupled VCO, simulations of phase shift according to Process, Voltage, Temperature (PVT) variations and mismatches are performed for f_{01} = 6.22 GHz, f_{02} = f_{03} = 6.15 GHz and f_{04} = 6.08 GHz. The simulations results are summarized in Tables 5,6,7 and 8.

Table 5 : Phase shift variation as a function of temperature

T= -40 °C	$\Delta\phi = 28.18°$
T= 27 °C	$\Delta\phi = 28.8°$
T= 80 °C	$\Delta\phi = 25.86°$

Table 6: Phase shift variation as a function of the process

High_was	$\Delta\phi = 24°$
Nominal	$\Delta\phi = 28.8°$
Low_was	$\Delta\phi = 27.55°$

Table 7: Phase shift variation as a function of the supply voltage

Vdd= 2.2 V	$\Delta\phi = 27.06°$
Vdd= 2.5 V	$\Delta\phi = 28.8°$
Vdd= 3 V	$\Delta\phi = 28.2°$

Table 8: Phase shift variation as a function of resistor mismatch

Mismatch =0%	$\Delta\phi = 28.21°$
Mismatch =5%	$\Delta\phi = 28.82°$
Mismatch =7%	$\Delta\phi = 29°$
Mismatch =10%	$\Delta\phi = 29.45°$

The results show that the phase shift hardly changes with PVT variations and mismatches showing the robustness of the proposed array made of four coupled differential VCOs.

IV. CONCLUSION

This paper described the design and the implementation of an array of four differential NMOS VCOs coupled through a resistive network, operating at 6 GHz and integrated in a 0.25 µm BICMOS SiGe process. The optimization in terms of phase noise of a single LC-VCO structure with a graphical optimization approach while satisfying design constraints has been presented. The proposed coupled-oscillators array achieves a simulated phase noise of -127.3 dBc/Hz at 1 MHz frequency offset from a 6 GHz carrier, while drawing 125 mA from a 2.5 V supply voltage giving a simulated phase progression that was continuously variable over the range $-64° < \Delta\phi < 64°$ and $-116° < \Delta\phi < 116°$.

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